UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,529	02/08/2002	Michael Richard Betker	7-1-3-12-5	2912

7590 12/22/2004

Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

EXAMINER	
RAMPURIA, SATISH	
ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 12/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/072,529	BETKER ET AL.	
	Examiner	Art Unit	
	Satish S. Rampuria	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the application filed on 02/08/2002.

2. Claims 1-12 are pending.

Specification

3. The abstract of the disclosure is objected to because it contains more than 150 words.

Correction is required. See MPEP § 608.01(b).

Appropriate correction is required

Drawings

4. The drawings were received on 05/01/2002. These drawings are acceptable by the examiner.

Claim Rejections - 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 1-10 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claims are non-statutory because they recite software components of implementing a software breakpoint, representing functional descriptive material without a computer readable medium or computer implemented method, program per se are not tangibly embodied. Claims 1-10 thus amounts to only abstract idea and are nonstatutory.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Publication No. 2002/0100024 to Hunter et al. (hereinafter called Hunter) in view of US Patent No. 6,615,368 to Dunlap (hereinafter called Dunlap).

Per claim 1, 3, 6, 8, 9, 10:

Hunter disclose:

- A method of implementing a software breakpoint in a multiprocessor system having a plurality of processors each coupled to a main memory (page 1, paragraph 6 "maintaining coherency of software breakpoints in shared memory when debugging a multiple processor system"), each of the processors having an instruction cache associated therewith (page 1, paragraph 6 "a software breakpoint in a shared memory location"), the method comprising the steps of:
- retrieving an instruction, for which the breakpoint is to be inserted, from a corresponding instruction address in the main memory (page 1, paragraph 7 "software breakpoint instruction is written to the shared memory location");
- inserting a breakpoint code at the instruction address in main memory (Fig. 13A elements 1304 and 1306 and related discussion); and

- after the breakpoint code is executed by a given one of the processors (page 7, paragraph 83 "resuming execution after hitting a breakpoint in common shared memory"), storing the retrieved instruction in the corresponding instruction cache for that processor (page 1, paragraph 7 "software breakpoint maintained for the located processors is updated to reflect that software breakpoint is being set at the shared memory location") and such that subsequent attempts by the given processor to access the instruction as stored in the instruction cache will cause the processor to retrieve the breakpoint code at the instruction address in main memory (page 1, paragraph 7 "software breakpoint instructions is written to the shared memory location... software breakpoint is cleared in shared memory, the original instruction stored").

Hunter does not explicitly disclose setting a use-once indicator associated with the instruction as stored in the corresponding instruction cache for that processor, wherein the use-once indicator, when set for the instruction as stored in the instruction cache, is operative via cache control logic to clear a validity indicator associated with the instruction after a single fetch of the instruction from the instruction cache.

However, Dunlap discloses in an analogous computer system setting a use-once indicator associated with the instruction as stored in the corresponding instruction cache for that processor (368col. 3, lines 27-29 "executing the debugging instruction enables a selected flag in the data processor"), wherein the use-once indicator, when set for the instruction as stored in the instruction cache (col. 6, lines 42-44 "COF address... detects the COF flag and loads the next instruction address... to external devices"), is operative via cache control logic to clear a validity

indicator associated with the instruction after a single fetch of the instruction from the instruction cache (368col. 6, lines 46-48 "the next instruction address is stored... sent to decode/dispatch logic... uses it to fetch the new instruction from the new branch").

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the method of setting a flag for the software breakpoint in the memory as taught by Dunlap into the method of implementing software breakpoint in a shared memory system as taught by Hunter. The modification would be obvious because of one of ordinary skill in the art would be motivated to have flags in a software breakpoint method to provide an optimize technique for debugging as suggested by Dunlap (col. 1, lines 51-61).

Per claim 2:

The rejection of claim 1 is incorporated, and further, Hunter disclose:

- wherein the instruction cache includes a plurality of sets of instruction information (page 8, paragraph 85 "debugging a multiple processor system with common shared instruction memory"), each corresponding to a particular instruction (page 8, paragraph 85 "a software memory map is created"), a given one of the sets of instruction information comprising the validity indicator, the use-once indicator, an instruction tag, and instruction data (page 8, paragraph 85 "memory map are indications as to whether or not the shared memory locations contain program instructions and whether or not a processor has an instruction cache").

Per claim 4:

The rejection of claim 1 is incorporated, and further, Hunter disclose:

- wherein the cache control logic is operative to compare portions of the instruction address to corresponding portions of instruction information as stored in the instruction cache and checks the validity indicator in determining if there is a hit or a miss between the instruction address and the instruction information as stored in the instruction cache (page 8, paragraph 88 "invalidation of different types of caches... used for mapping virtual memory addresses to physical addresses..." and page 7, paragraph 83 "a check is made to determine if there is a request to step over a software breakpoint in common shared memory or resume execution after hitting a breakpoint in... memory").

Per claim 5:

The rejection of claim 1 is incorporated, and further, Hunter does not explicitly disclose wherein the use-once bit when set, being operative via the cache control logic to clear the validity indicator associated with the instruction as stored in the instruction cache after a single fetch of the instruction from the instruction cache, thereby automatically causes a miss between the instruction address and the instruction as stored in the instruction cache when the given processor attempts to retrieve the instruction from the instruction cache subsequent to the single fetch.

However, Dunlap discloses in an analogous computer system wherein the use-once bit when set, being operative via the cache control logic to clear the validity indicator associated with the instruction as stored in the instruction cache after a single fetch of the instruction from the instruction cache (col. 6, lines 40-45 "functional units determines that a change of flow (COF)... flag is set... detects the active COF flag and loads the next instruction address... to

external devices"), thereby automatically causes a miss between the instruction address and the instruction as stored in the instruction cache when the given processor attempts to retrieve the instruction from the instruction cache subsequent to the single fetch (col. 6, lines 46-50 "next instruction address is stored... sent to instruction decode/dispatch logic... uses fetch instruction from new branch... processing continues").

The feature of using use-once bit to clear the validity indicator would be obvious for the reasons set forth in the rejection of claim 1.

Per claim 7:

The rejection of claim 1 is incorporated, and further, Hunter disclose:

- wherein the validity indicator associated with the instruction comprises a single bit stored in a given set of the instruction cache (page 7, paragraph 78 "invalidation of different types of caches including instruction cashes, data caches... used for mapping... physical addresses").

Claims 11 and 12 are the system and computer program product claims respectively corresponding to method claim 1 and rejected under the same rational set forth in connection with the rejection of claim 1 above.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Satish S. Rampuria** whose telephone number is **(571) 272-3732**. The examiner can normally be reached on **8:30 am to 6:00 pm**.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Kakali Chaki** can be reached on **(571) 272-3719**. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Satish S. Rampuria
Patent Examiner
Art Unit 2124
12/13/2004

KAKALI CHAKI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100